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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,916	APPLEYARD ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,10-14,16-18 and 20* is/are rejected.

7)☒ Claim(s) *5,9,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto et al. (U.S. Pat. No. 6515548).

In regard to claim 1:

Matsumoto et al. teach a method of testing and measuring an IC (integrated circuit) chip (see Abstract and col. 1, lines 10-18), comprising: prior to manufacturing, determining a change of a temperature sensitive parameter of the chip, that is predictable with change of temperature (Fig. 2; col. 5, lines 49-54; cols. 6-8, lines 27-47); during manufacturing, measuring the temperature sensitive parameter of the chip during testing of the chip, measuring the chip temperature during or following the measurement of the temperature sensitive parameter, determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature (cols. 8-10, lines 54-36).

In regard to claims 3 and 4:

Matsumoto et al. also teach: determining a change of the temperature sensitive parameter of the chip that is the chip maximum operating frequency Fmax (col. 1, lines 11-18 and cols. 2-3, lines 52-8); measuring the chip temperature with an on-chip diode (col. 5, lines 31-48).

In regard to claim 11:

Matsumoto et al. further teach: a method of testing and measuring an IC (integrated circuit) chip (see Abstract and col. 1, lines 10-18), comprising: determining a change of a temperature sensitive parameter of the chip, that is predictable with change of temperature, with temperature (Fig. 2; col. 5, lines 49-54; cols. 6-8, lines 27-47); measuring the temperature sensitive parameter of the chip during testing of the chip, measuring the chip temperature during or following the measurement of the temperature sensitive parameter, determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature (cols. 8-10, lines 54-36).

In regard to claims 13 and 14:

Matsumoto et al. further teach: determining a change of the temperature sensitive parameter of the chip that is the chip maximum operating frequency Fmax (col. 1, lines 11-18 and cols. 2-3, lines 52-8); measuring the chip temperature with an on-chip diode (col. 5, lines 31-48).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2, 10, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (U.S. Pat. No. 6515548) in view of Abercrombie (U.S. Pub. No. 20030208286).

Matsumoto et al. teach the method that includes the subject matter discussed above. Matsumoto et al. do not mention expressly that: regarding claims 2 and 12, sorting the chip into a category based upon the adjusted temperature sensitive parameter of the chip; regarding claims 10 and 20, testing the chip in production tests to classify each chip into different categories of the temperature sensitive parameter.

Abercrombie discloses a method of manufacturing integrated circuits, and teaches: sorting integrated circuit chip into a category based upon a temperature sensitive manufacturing parameter of the chip (sections 0032, 0036 and 0038); and testing the chip in production tests to classify each chip into different categories of the temperature sensitive parameter (sections 0032, 0036 and 0038).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Abercrombie in the invention of Matsumoto et al. in order to correlate process parameter variations to individual sources of those variations and further manage the manufacturing process (Abercrombie, see

Abstract and section 0010).

5. Claim 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (U.S. Pat. No. 6515548) in view of Syed (U.S. Pub. No. 20050022081).

Matsumoto et al. teach the method that includes the subject matter discussed above. Matsumoto et al. do not mention expressly: regarding claims 6 and 16, determining a change of the temperature sensitive parameter of the chip that is the chip power consumption; regarding claims 7 and 17, determining a change of the temperature sensitive parameter of the chip that is the chip I (input)/0 (output) timings; regarding claims 8 and 18, determining maximum and minimum voltage tests which measure the highest and lowest possible voltages at which a product will operate.

Syed discloses test systems for testing integrated circuit devices and to calibration associated systems and methods, and teaches: determining a change of the temperature sensitive parameter of the chip that is the chip power consumption (sections 0008, 0009 and 0012); determining a change of the temperature sensitive parameter of the chip that is the chip I (input)/0 (output) timings (sections 0009, 0020 and 0160-0162); and determining maximum and minimum voltage tests which measure the highest and lowest possible voltages at which a product will operate (sections 0003, 0008 and 0020).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Syed in the invention of Matsumoto et al. in order to test integrated circuits that are suitable for high-speed and high accuracy

timing applications and that are low cost and have small size and low power consumption relative to conventional systems (Syed, section 0012).

Allowable Subject Matter

6. Claims 5, 9, 15 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

7. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claims 5 and 15 is the inclusion of the claimed method step of measuring the chip temperature with the on-chip diode by forcing a current through the on-chip diode, measuring the diode voltage at the start of test when the temperature during test Tdtest is known, and measuring the diode voltage again after the Fmax test when the temperature Tdtest is unknown, and using the measurements to determine a predicted Fmax at Tmax, based upon which the part is sorted into speed categories. It is this limitation found in each of the claims, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claims 9 and 19 is the inclusion of the claimed method step of testing the chip in preproduction tests to provide a realistic indication of speed at Tmax for performance modeling purposes to predict the speed of

chips and the percentages of good/operative chips sorted into speed categories. It is this limitation found in each of the claims, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Arguments

9. Applicant's arguments filed 08/03/05 have been fully considered but they are not persuasive.

In regard to independent claims 1 and 11, Applicant argued that "Matsumoto does not teach determining a temperature sensitive parameter of the chip that is predictable with change of temperature". The Examiner's position is that the Matsumoto patent does teach this limitation. As admitted by the Applicant, Matsumoto teaches determining how the oscillator frequency response will behave as a function of the temperature (page 11, 2nd paragraph). This is an obvious equivalence of determining a temperature sensitive parameter of the chip that is predictable with change of temperature. Specifically, if the oscillator frequency response is a function of the temperature, then there must be a deterministic relationship between the oscillator frequency response and the temperature. That is, as agreed by the Applicant (page 12, 1st paragraph), if one of the parameter is known, the other can be determined, i.e., the relationship is predictable.

Applicant also argued that "Matsumoto also does not teach or suggest, during manufacturing, determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature". The Examiner's position is that the Matsumoto patent does teach this method step. Although Matsumoto executes the adjustment in a calibration step, it is deemed to be during a manufacture phase, considering that it is common in the manufacturing industry that a calibration step is

carried out right after the manufacturing step at the manufacturer site, therefore, can be treated as a part of the manufacture process.

The rest of the Applicant's arguments regarding the dependent claims are reliant upon the two issues discussed above, and are deemed to be non-persuasive as well for the reasons provided above for independent claims 1 and 11.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

XS
October 10, 2005

BRYAN BUI
PRIMARY EXAMINER